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EXAMINER	
SHECHTMAN, SEAN P	
ART UNIT	**PAPER NUMBER**
2125	3

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/824,301	Applicant(s) BODE ET AL.	
	Examiner Sean P. Shechtman	Art Unit 2125	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 November 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 April 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Information Disclosure Statement

1. The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A(1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered. See page 7, lines 13-20 of the instant specification.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "80" has been used to designate both a process controller and a tool controller (See page 11, lines 9-20). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. 35 U.S.C. 112, first paragraph, requires the specification to be written in "full, clear, concise, and exact terms." The specification should be revised carefully in order to comply with 35 U.S.C. 112, first paragraph. Examples of some unclear, inexact or verbose terms used in the specification are:

It is unclear how the qualification process of the first embodiment (page 10, lines 13-14) may be reduced in scope compared to a full scale tool qualification process. Applicant fails to

describe a full scale tool qualification process, and therefore applicant fails to describe the claimed qualification process that reduces the scope of the full scale tool qualification process.

4. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

The specification is objected to as failing to provide proper antecedent basis for claims 3-4, 7-10, 12-16, 18-20, 23-27, 32-34, 35, 37-45.

For example, referring to claim 4, the specification is objected to as failing to provide proper antecedent basis for "a deposition tool adapted to planarize a semiconductor wafer" and "estimating the control variable value includes estimating a material removal rate".

For example, referring to claim 8, the specification is objected to as failing to provide proper antecedent basis for "a photolithography stepper adapted to expose a photoresist layer on a semiconductor wafer" and "performing the qualification procedure comprises processing a test wafer in the photolithography stepper to determine an overlay characteristic of the photolithography stepper".

For example, referring to claim 12, the specification is objected to as failing to provide proper antecedent basis for "a polishing tool having at least one polishing pad adapted to planarize a semiconductor wafer" and "receiving the tool event notification comprises receiving a notification when the polishing pad is replaced".

5. The examiner has provided a number of examples of the specification deficiencies in the above, however, the list of deficiencies may not be all inclusive. Applicant should refer to these

as examples of deficiencies and should make all necessary corrections to eliminate the specification objections.

Claim Objections

6. Claims 3-5, 7-10, 12-16, 18-21, 32-34, 36-40 are objected to because of the following informalities:

The phrase "estimating the control", claim 3, page 13, line 15, should be rephrased "said tool controller estimating the control".

Claims 4-5, 32-34 are objected to because of the same reason given above.

The phrase "performing the qualification", claim 7, page 14, line 8, should be rephrased "said tool controller performing the qualification".

Claims 8-10, 18-21, 37-40 are objected to because of the same reason given above.

The phrase "receiving the tool event", claim 12, page 15, line 6, should be rephrased "said tool controller receiving the tool event".

Claims 13-16, 23-27 are objected to because of the same reason given above.

The phrase "a deposition tool", claim 4, should be rephrased "a polishing tool".

The phrase "tool is adapted", claim 36, should be rephrased "tool controller is adapted".

Appropriate correction is required.

7. Due to the number of claim objections, the examiner has provided a number of examples of the claim deficiencies in the above objections, however, the list of objections may not be all inclusive. Applicant should refer to these objections as examples of deficiencies and should make all the necessary corrections to eliminate the claim objection problems and place the claims in proper format.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1, 6, 17, and 28, are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,886,896 to Lantz.

Referring to claims 1, 6, 17, and 28, Lantz discloses a computer controller that provides an automatic setup (initializing) of a processing tool (Abstract). Wherein the tool is adapted to process wafers (See Fig. 3, Col. 1, lines 8-12).

The computer controls the manufacturing process of the processing tool according to a set of process instructions (i.e., control algorithm), and a memory stores and associates identification data, which identifies the semiconductor devices on which the manufacturing process step is performed by the processing tool (Col. 2, lines 10-22). Examiner asserts that such a process step is a tool event.

The system has ability to set up (qualification procedure) a control value (i.e., control variable) of the sensor so that the computer can stop the process performed by the processing tool automatically if the data from the sensor indicates this to be the proper course of action (Col. 2, lines 42-49).

The control of the processing tool by the computer is performed according to a single recipe (Abstract).

According to Lantz, the equipment interface, and specifically the equipment logic server, forms a message to send to the recipe management system 34 in step 58 (i.e., receiving tool event notification). The recipe management system 34, in step 60, examines the message and produces a single recipe comprising a dual linked recipe for controlling both the processing tool 16 (i.e., initializing) and the sensor arrangement 24. This recipe is provided back to the equipment interface 32 (Col. 5, lines 53-60). Examiner asserts that the computer then controls the manufacturing process of the processing tool according to a set of process instructions (i.e., control algorithm),

wherein the computer includes a manufacturing execution system that sends control signals to the processing tool and equipment interface, and

wherein the equipment interface generates said process instructions according to a recipe (Claim 1).

Referring to claims 1, 6, and 17, examiner would like to note that the claims do not specify where the tool event notification is received or sent from, where and how the tool recipe is provided, or where and how the tool controller is initialized. Therefore, the claim limitations are believed to be met.

Referring to claim 28, examiner would like to note that the claims do not describe where the tool event notification is sent from, where or how the tool recipe is provided, or where the tool controller is initialized. Therefore, the claim limitations are believed to be met.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,886,896 to Lantz.

Referring to claim 29, according to Lantz the equipment interface 32, and specifically the equipment logic server 36, forms a message to send to the recipe management system 34 in step 58 (i.e., receiving tool event notification). The recipe management system 34, in step 60, examines the message and produces a single recipe comprising a dual linked recipe for controlling both the processing tool 16 (i.e., initializing) and the sensor arrangement 24. This recipe is provided back to the equipment interface 32 (Col. 5, lines 53-60). Col. 3 lines 36-51 describe the embodiment where a single computer serving as the shop floor system controller may also act as the computer for each of the different processing stations. Therefore, examiner submits that this single computer acts as a process control server. The computer contains an equipment logic server which sends a message to the recipe management system which then provides the recipe back to the equipment interface which is used in generating (i.e., sending) the instructions executed by the execution system (i.e., tool controller).

If a process control server sending the tool event notification to the tool controller is not clear, then it would have been obvious to one of ordinary skill in the art at the time that the invention was made to omit the recipe management system of Lantz, wherein the equipment interface (consisting of a server) incorporates the functions of the recipe management system and generates (i.e., sends) the set of process instructions in accordance with a recipe to the execution system for controlling the processing tool, since it has been held that omission of an element and

its function in a combination where the remaining elements perform the same functions as before involves only routine skill in the art. *In re Karlson*, 136 USPQ 184.

10. Claims 1, 6, 11, 17, 22, 28, 29, and 30, are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,432,702 to Barnett, and further in view of U.S. Patent No. 6,442,445 to Bunkofske.

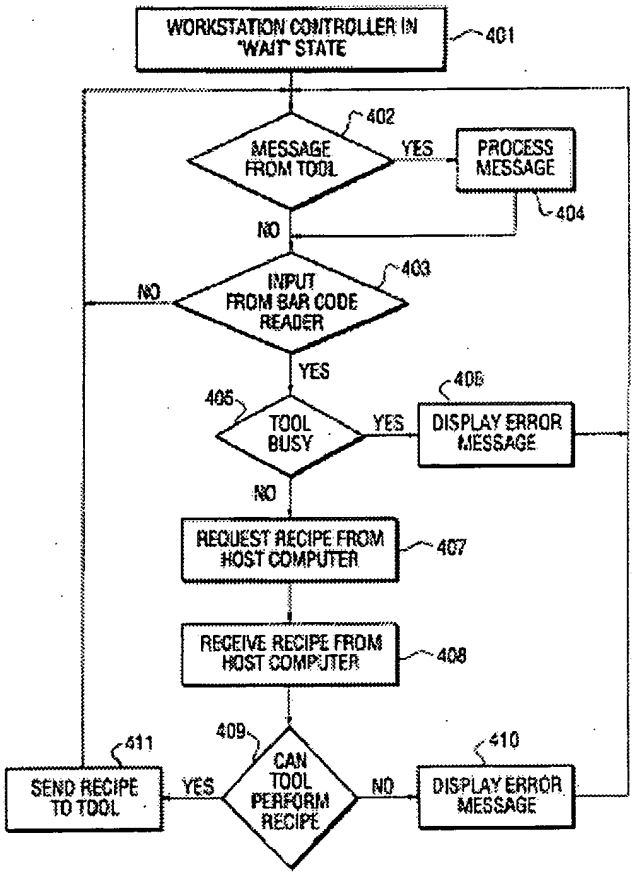
Referring to claims 1, 6, 17, 28, and 29, Barnett teaches a workstation/tool controller, wherein if the process can be performed by the tool, the recipe is sent to the tool so that the tool has the information it needs to process the wafer (Abstract). Examiner submits that the determining of whether or not the process can be performed by the tool is a qualification procedure.

The tool 10 performs a process (i.e. a recipe consisting of a sequence of process steps typically relating to temperature, pressure, gas, flow, etc.) on a wafer (Col. 2, lines 33-48).

The tool 10 may be provided the details of the recipe externally, e.g. from the workstation controller 30 (Col. 2, lines 33-48). Examiner asserts that the workstation controller is a process server and the details of the recipe (the recipe being a series of steps in the processing of the wafers by processing tools) are tool event data.

The host computer sends information (i.e., tool event data) to the workstation controller (Col. 3, lines 55-66). Furthermore, the flow chart in figure 4 below shows that the workstation controller 30 is in a wait state 401, where it waits for messages in step 402 from the tool (Col. 4, lines 23-52).

FIG. 4



Barnett also teaches that software and hardware is used together to form a bridge between the tool and host computer which controls the fabrication process (Col. 3, lines 12-22).

If initializing is not clear, then Bunkofske teaches analogous art wherein, each time an item is processed by a tool, the raw data (e.g., a time series of a large set of process parameters) is input to an initialized module that has directories which have been set. In addition, a predetermined time series transformation program and reference statistics are also input. Bunkofske teaches including a unique transformation program and reference statistics for each product recipe (e.g., there may be distinct recipes for different products and technologies run on a given manufacturing tool) (Col. 7, lines 54-65 of '445). Furthermore, examiner asserts that a

time series of a set of process parameters is tool event data (See also Col. 7, lines 1-12 of '445 for referencing what Bunkofske teaches as raw data).

Referring to claims 11, 22, and 30, Bunkofske teaches a method and apparatus for multivariate tool fault detection to prevent wafer mis-processing (Col. 5, lines 16-39 of '445).

Therefore, it would have been obvious to one of ordinary skill in the art at the time that the invention was made to combine the teachings of Barnett and Bunkofske to include the initializing and preventive maintenance of Bunkofske.

One of ordinary skill in the art would have been motivated to combine these references because Bunkofske teaches that the invention uses human expertise to distinguish between which variations can be tolerated and which variations are of interest (Col. 5, lines 29-31 of '445). Furthermore, Bunkofske teaches that the invention inhibits the use of a tool until corrective action is taken, and also monitors process recipes for changes to see if those changes are authorized or unauthorized (Col. 12, lines 4-11 of '445).

11. Claims 2 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over **either** U.S. Patent No. 5,886,896 to Lantz **or** the combination of Barnett and Bunkofske (U.S. Patent No. 5,432,702 to Barnett and U.S. Patent No. 6,442,445 to Bunkofske) as applied to claims 1 and 28 above, and further in view of U.S. Patent No. 6,041,270 to Steffan.

Referring to claims 2 and 31, neither Lantz nor the combination of Barnett and Bunkofske teach estimating a control variable.

Referring to claims 2 and 31, Steffan teaches manufacturing semiconductor wafers using a simulation (i.e., estimation) tool to determine a set of predicted wafer electrical test

measurements (i.e., estimation of a control variable) that are compared to a set of target wafer electrical test measurements to obtain a set of optimized process parameters for the equipment for the next process (Abstract of '270).

The predicted wafer electrical test (WET) measurements may provide a widened process control window (i.e., control algorithm). This means, for example, that a parameter that is currently being measured may be adjusted (i.e., initialized based on WET measurements) to compensate for a parameter that has been previously measured and was either within or without that parameters specification (Col. 3, lines 63 – Col. 4 of '270).

Therefore, it would have been obvious to one of ordinary skill in the art at the time that the invention was made to combine the teachings of **either** U.S. Patent No. 5,886,896 to Lantz **or** the combination of Barnett and Bunkofske (U.S. Patent No. 5,432,702 to Barnett and U.S. Patent No. 6,442,445 to Bunkofske) with the simulation tool of Steffan.

One of ordinary skill in the art would have been motivated to combine **either** Lantz **or** the combination of Barnett and Bunkofske with the teachings of Steffan because of the following reasons:

Steffan teaches that the optimized process parameters are compared to the equipment characteristics for the equipment of the next process and the process parameters for the next process are automatically adjusted (Abstract of '270).

The widened process control window provides more flexibility to the process control engineer to continue processing a wafer lot and can result in cost savings by not having to scrap wafer lots that can be saved by merely adjusting subsequent process parameters (Col. 4, lines 20-30 of '270).

The simulation tool allows for the specific targeting of wafer lots to achieve selected performance characteristics, provides critical information to process engineers for the disposition decision for wafer lots if manufacturing specification targets are not met, and it allows for the widening of process specification limits based on data from previous process and layer data and the current tool performance characteristics (Col. 4, line 65 – Col. 5, line 9 of '270).

12. Claims 11, 22, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over either U.S. Patent No. 5,886,896 to Lantz as applied to claims 1, 17, and 28 above, and further in view of U.S. Patent No. 6,041,270 to Steffan.

Referring to claims 11, 22, and 30, if calibration (i.e., setup of tools) in Lantz is unclear, Steffan teaches the statistical manufacturing simulation also includes calibration simulation data. The calibration simulation data has input from a comparison made of the predicted WET measurements and the collected WET data from all previous process steps (Col. 4, lines 1-15 of '270). Examiner asserts that such simulation occurs after the wafer lot is started, and thereby could easily be considered a tool event notification itself or within any of the tool event notifications described in Lantz above.

Therefore, it would have been obvious to one of ordinary skill in the art at the time that the invention was made to combine the teachings of Lantz with the calibration simulation tool of Steffan.

One of ordinary skill in the art would have been motivated to combine these references because, Steffan's invention allows for the maintenance of tight process control based on previous process or layer history (Col. 5, lines 1-2 of '270).

13. Claims 35 and 36, are rejected under 35 U.S.C. 103(a) as being unpatentable over **either** U.S. Patent No. 5,886,896 to Lantz **or** the combination of Barnett and Bunkofske (U.S. Patent No. 5,432,702 to Barnett and U.S. Patent No. 6,442,445 to Bunkofske) as applied to claim 28 above, and further in view of U.S. Patent No. 6,303,395 to Nulman.

Referring to claims 35 and 36, neither Lantz nor the combination of Barnett and Bunkofske teach scheduling a qualification procedure.

However, Nulman teaches analogous art with a scheduling system (Abstract of '395), wherein the scheduling system schedules additional wafers for processing or maintenance activities (i.e., qualification procedure) (Col. 7, lines 9-40 of '395). Examiner asserts that the manufacturing execution system (MES) of Nulman provides for a scheduling controller of chamber manufacturing environment that receives inputs from MES scheduling environment to control wafer inventory consumables, maintenance parts, maintenance activities and facilities systems scheduling. For example scheduling the electrical power needed for executing the manufacturing process within the chamber (i.e., scheduling in response to tool event of electrical power needed for executing process). MES scheduling environment coordinates scheduling of various other functions or activities as well. For example, maintenance activities scheduling is coordinated with chamber status controller (i.e., tool controller), such as scheduling the status of the chamber off-line for maintenance activities or scheduling wafer inventory and consumables such as process gas in coordination with an on-line in-process status (Col. 8, lines 23-43 of '395).

Therefore, it would have been obvious to one of ordinary skill in the art at the time that the invention was made to combine the teachings of **either** Lantz **or** the combination of Barnett and Bunkofske with the scheduling system of Nulman.

One of ordinary skill in the art would have been motivated to combine Lantz **or** the combination of Barnett and Bunkofske with the teachings of Nulman because,

Nulman teaches the wafer fab is provided with a novel wafer fab efficiency system employing an algorithm for more efficient scheduling of wafer fab resources, resulting in a more efficient wafer flow and thus maximizing die output and wafer fab utilization (Col. 4, lines 6-11 of '395).

14. Claims 3-5, 7-10, 12-16, 18-21, 23-27, 32-34, and 37-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over "Semiconductor Manufacturing Technology" by Michael Quirk.

Referring to claims 3-5, 7-10, 12-16, 18-21, 23-27, 32-34, and 37-45. Lantz teaches an example of processing tool as an etch tool or a deposition tool (Col. 3 of '896) and a processing tool chamber (Col. 1, lines 31-38), although these processing tools are given merely as examples. Barnett further teaches the tools that process the wafer are deposition and etching tools (Col. 2, lines 33-49 of '702). Bunkofske refers to a chamber cleaning maintenance activity in Col. 5, lines 32-40.

U.S. Patent No. 6,303,395 to Nulman filed June 1st, 1999, teaches (in the background of the invention) similar processes commonly known in wafer fab such as oxidation, etching, deposition, planarization, and cleaning (Col. 1, lines 17-29 of '395). According to Nulman, it is

well known to those of ordinary skill in the art that one or more processing parameters of a typical wafer fab process step need to be controlled to obtain desired process characteristics, wherein the target value for these control limits are determined from a test wafer (Col. 2, lines 1-25 of '395). Nulman teaches a cleaning chamber and monitoring of rates of wafer fab tools such as the deposition tool in the background of the invention (Col. 1, lines 43-68, Col. 2, lines 1-25 of '395).

Although the references cited above fail to meet the limitations of every tool claimed in claims 3-5, 7-10, 12-16, 18-21, 23-27, 32-34, and 37-45, examiner submits that the disclosure of "Semiconductor Manufacturing Technology" by Michael Quirk does meet the limitations of every tool claimed by applicant, and therefore having been written and published prior to applicant having applied for a patent, examiner asserts that such information was commonly known in the art. Examiner has supplied applicant with two copies of the same book. Examiner notes that the two copies of the book being supplied for the rejection have an excellent table of contents which can easily lead to the detailed description required to support those tools claimed. One of the copies of the book has highlighted most of the words of the respective tools, and the other copy of the book contains those illustrations not readable in the HTML format required to highlight the respective terms seen in the first copy.

The patentable invention is not the tool that the tool controller uses, therefore since Lantz teaches only examples of tools used (Col. 3 of '896) and Steffan teaches that the system evaluates the trend of each processing tool (i.e., processing tools used in wafer fabrication) (Col. 2, lines 58-65 of '270), it is inherent that said tool controller could use any of the tools described above or in the references cited as commonly known in the art.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to an Advanced Process Control Systems for Semiconductor Wafer Manufacturing.

"Advanced Process Control Systems Description of an easy-to-use control system incorporating pluggable modules", by Fukuda.

The following publications are cited to further show the state of the art with respect to a semiconductor manufacturing system with maintenance scheduling and processing tool controls according to a programmed recipe.

U.S. Pub. No. 2002/0116083 A1 to Schulze.

The following patents are cited to further show the state of the art with respect to photolithography.

U.S. Pat. No. 5,861,320 to Shiraishi (See Col. 14, lines 1-15).

The following patents are cited to further show the state of the art with respect to etching tools in a semiconductor wafer processing.

U.S. Pat. No. 5,920,796 to Wang et al.

The following patents are cited to further show the state of the art with respect to controlling semiconductor fabrication tools.

U.S. Pat. No. 6,197,604 to Miller et al.

U.S. Pat. No. 6,521,466 to Castrucci.

The following publications are cited to further show the state of the art with respect to preventive maintenance in semiconductor wafer processing tool.

U.S. Pub. No. 2002/0055801 A1 to Reiss et al.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sean P. Shechtman whose telephone number is (703) 305-7798. The examiner can normally be reached on Monday-Friday from 9:30am to 6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo P. Picard, can be reached on (703) 308-0538. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-9600.

SPS

Sean P. Shechtman

April 28, 2003

LEO PICARD
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100